

What is claimed is:

- 1 1. An assembly, comprising:
2 a die, the die having a body comprising a first material; and
3 an interposer having a first side and a second side, the die coupled to the
4 first side of the interposer;
5 wherein the interposer comprises the first material, and the first side is
6 electrically and mechanically coupled to the die.
- 1 2. The structure of Claim 1, further comprising circuit elements embedded
2 within the interposer.
- 1 3. The structure of Claim 2, wherein circuit elements comprise capacitors.
- 1 4. The structure of Claim 2, wherein circuit elements comprise transistors.
- 1 5. The structure of Claim 1, wherein capacitors and transistors are
2 incorporated into the interposer.
- 1 6. The structure of Claim 1, further comprising a circuit substrate coupled to
2 the second side of the interposer.

1 7. The structure of Claim 6, wherein the die is coupled to the interposer by
2 solder bumps, and the interposer is coupled to the circuit substrate by solder .
3 balls.

1 8. The structure of Claim 7 wherein the solder bumps have a first pitch, the
2 solder balls have a second pitch, and the second pitch is greater than the first
3 pitch.

1 9. The structure of Claim 1, wherein the interposer has a first interconnection
2 pitch on the first side, and a second interconnection pitch on the second side,
3 and the second interconnection pitch is greater than the first interconnection
4 pitch.

1 10. An assembly comprising:
2 an integrated circuit formed on a silicon substrate;
3 an interposer having a first surface and an opposing second surface; and
4 a circuit substrate;
5 wherein the interposer is disposed between the integrated circuit and the
6 circuit substrate, and the interposer comprises silicon.

1 11. The assembly of the Claim 10, wherein the interposer is electrically and
2 mechanically coupled to the integrated circuit.

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1 12. The assembly of Claim 11, wherein the interposer is coupled to the
2 integrated circuit by a plurality of solder bumps.

1 13. The assembly of Claim 11, wherein the interposer is coupled to the circuit
2 substrate by a plurality of solder balls.

1 14. The assembly of Claim 10, further comprising electrical circuits
2 incorporated into the interposer.

1 15. The assembly of Claim 14, wherein the electrical circuits comprise
2 electrostatic discharge protection circuits.

1 16. The assembly of Claim 14, wherein the electrical circuits comprise buffer
2 circuits.

1 17. The assembly of Claim 14, wherein the electrical circuits comprise
2 memory circuits.

1 18. An electronic assembly comprising:
2 a die having a silicon substrate;
3 an interposer having a silicon substrate with a first surface and an
4 opposing second surface, the first surface attached to the die by solder bumps;
5 and

6 a circuit substrate attached to the second surface by solder balls;
7 wherein the interposer comprises circuit elements.

1 19. The electronic assembly of Claim 18, wherein the circuit elements
2 comprise active circuit elements.

1 20. The electronic assembly of Claim 18, wherein the circuit elements
2 comprise passive circuit elements.

1 21. The electronic assembly of Claim 18, wherein the circuit elements
2 comprise active and passive circuit elements.

1 22. The electronic assembly of Claim 21, wherein the active circuit elements
2 include at least one field effect transistor, and the passive circuit elements
3 include at least one capacitor.

1 23. The electronic assembly of Claim 18, wherein the die comprises a first
2 plurality of insulated gate field effect transistors having a first set of electrical
3 characteristics, the interposer comprises a second plurality of insulated gate field
4 effect transistors having a second set of electrical characteristics, and the first
5 set of electrical characteristics are different from the second set of electrical
6 characteristics.

1 24. The electronic assembly of Claim 23, wherein the first set of electrical
2 characteristics includes a first gate dielectric breakdown voltage, the second set
3 of electrical characteristics includes a second gate dielectric breakdown voltage
4 and the second gate dielectric breakdown voltage is greater than the first gate
5 dielectric breakdown voltage.

1 25. The electronic assembly of Claim 18, wherein the die and the interposer
2 are electrically coupled through the solder bumps, and a first power supply node
3 of the die is coupled to a first terminal of a capacitor disposed on the interposer,
4 and a second power supply node of the die is coupled to a second terminal of
5 the capacitor.

1 26. A method of making an electronic assembly, comprising:
2 coupling an integrated circuit (IC) and an interposer; and
3 coupling a circuit substrate and the interposer;
4 wherein the IC and the interposer each have a body substantially
5 comprising the same material, and wherein coupling comprises mechanically
6 attaching and electrically connecting.

1 27. The method of Claim 26, wherein the IC and the interposer each have a
2 body substantially comprising silicon, and wherein the circuit substrate comprises
3 a printed circuit board.

1 28. The method of Claim 26, further comprising forming circuit elements on
2 the interposer.

1 29. The method of Claim 26, further comprising incorporating circuit elements
2 into the interposer.

1 30. The method of Claim 29, wherein circuit elements comprise active and
2 passive circuit elements.

1 31. A method of making an interposer, comprising:
2 forming an oxide layer on each of a first surface and a second surface of
3 a substrate;
4 patterning the oxide layer of the first surface so as to expose portions of
5 the substrate;
6 isotropically etching through a first portion of the exposed substrate to
7 form a first portion of a deep-via opening;
8 anisotropically etching through a second portion of the exposed substrate
9 to form a second portion of a deep-via opening;
10 sputtering a copper barrier and a copper seed layer into the first and
11 second portions of the deep-via opening;
12 electroplating a conductive material over the seed layer to form a deep-
13 via; and

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- 14 forming vias and interconnect lines over the second surfac of the
15 substrate;
16 wherein at least one interconnect line is electrically coupled to at least
17 one deep-via.